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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID SHIPPY

Appeal 2008-3797
Application 10/821,025
Technology Center 2100

Decided:[1] April 29, 2009

Before JOHN C. MARTIN, JAY P. LUCAS, and
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Data (electronic delivery).

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-9 and 16-21. Claims 10-15 are cancelled. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Invention

Appellant's invention relates to a multi-thread processor architecture. More particularly, the invention relates to the operation of architected registers. (Spec. 1, ll. 5-7).

Representative Claims

1. An architected register file system at least configured to utilize a plurality of threads, comprising:

a plurality of register files, wherein each register file of the plurality of register files at least corresponds to a respective thread of the plurality of threads;

a plurality of Status and Control Registers (SCR), wherein each SCR corresponds to a respective thread of the plurality of threads; and

a plurality of control bit sets, wherein each control bit set corresponds to at least one SCR, and wherein each control bit set is at least configured to allow a thread associated with an associated SCR to utilize other register files associated with other threads.

16. A method for utilizing a plurality of register files in a multithread system, the method comprising:

receiving an instruction for a first thread having an operations code field, a write field, and one or more read fields, wherein the operations code field defines a desired operation for the instruction, wherein the write field defines an address location to which a result of the operation is to be stored, and wherein the at least one read field defines an address location from which data is to be read for the operation;

decoding the instruction;

setting a first status and control register associated with the first thread and a second status and control register associated with a second thread based on the decoding of the instruction, wherein a first register file is associated with the first thread and a second register file is associated with the second thread;

determining whether the first thread is permitted to utilize the second register file associated with the second thread based on at least one of the first status and control register or the second status and control register; and

if the first thread is permitted to utilize the second register file, performing the operation utilizing the second register file by writing to or reading from the second register file associated with the second thread.

Prior Art

The Examiner relies on the following reference:

Sollars	US 5,900,025	May 4, 1999

Examiner's Rejections

I. Claims 1-5, 7, 8, 16-21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sollars.

II. Claims 6 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sollars.

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Briefs and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellant. Arguments which Appellant could have made but did not make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

APPELLANT'S CONTENTIONS

1. Appellant contends that Sollars does not disclose the limitation of each operand register file corresponding to a respective thread. (App. Br. 7).
2. Appellant contends that Sollars does not disclose the limitation of a first register file that is associated with the first thread and a second register file that is associated with the second thread. (App. Br. 10-11).

ISSUE

We consider the following issue that flows from the contentions between the Appellant and the Examiner:

Has Appellant shown the Examiner erred in determining that Sollars discloses that the register files and the Status and Control registers correspond to a respective thread of the plurality of threads?

PRINCIPLES OF LAW

Anticipation

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. However, this is not an "ipsissimis verbis" test. *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990).

Obviousness

"What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007).

FINDINGS OF FACT

1. Sollars discloses that a thread is used to access and modify its own set of control registers. (Col. 3, ll. 45-48).

2. Sollars discloses a plurality of control register files, 20a and 20b. (Fig. 1 and col. 5, ll. 10-16 and col. 5, ll. 55-56).

3. Sollars discloses control register sets that control concurrent execution of multiple peer process threads. (Col. 2, ll. 2-6). Sollars also discloses that *control registers* support eight active threads. (Col. 2, ll. 10-11).

4. Sollars discloses a primary operand register file 22a. Sollars is silent with regards to the primary operand register file having associated threads or thread privileges. (See Col. 5, ll. 21-30).

ANALYSIS

Section 102 rejection of claims 1-5, 7, and 8

As discussed above, Appellant argues that Sollars fails to disclose the limitation of a plurality of register files, wherein each register file of the plurality of register files at least corresponds to a respective thread of the plurality of threads.

The Examiner argues that there are corresponding threads to the control registers and, since the control registers and operand registers are coupled together, the coupling is a form of correspondence. (*See* Ans. 11).

We note that the language of claim 1 requires that each register file of the plurality of register files and each Status and Control Register of the plurality of Status and Control Registers (SCR), must correspond to a respective thread of the plurality of threads. (Claim 1). Because claim 1 "allow[s] a thread associated with an associated SCR to utilize other register files associated with other threads," we understand the terms "corresponds to" and "associated with" in claim 1 to mean "assigned to" rather than "currently being used by." The same is true of the other independent claims.

As noted above, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. As discussed above, we find that Sollars discloses that the *control registers* support eight active threads. (See FF 3). We

further find that Sollars does not disclose that the operand registers (alleged by the Examiner as the plurality of register files) correspond in any way to the threads. (FF 3). The absence of the operand register's correspondence to any thread is sufficient to show that Sollars fails to anticipate the limitations of claim 1. Moreover, we find that even if the Primary and Secondary control register file 20a of Sollars, which has corresponding threads, was considered to be the claimed "plurality of register files," Sollars fails to disclose another plurality of register files that have corresponding threads, as required by the language of claim 1.

Based on the record before us, we find that Appellant has shown that the Examiner erred in determining that Sollars discloses register files and Status and Control registers that each corresponds to a respective thread of the plurality of threads, as required by the language of claim 1. Accordingly, we reverse the Examiner's rejection of claim 1 and dependent claims 2-5 as being anticipated by Sollars.

Independent claim 7 recites in pertinent part "a plurality of register files with associated SCRs . . . wherein each register file is at least associated with one thread of a plurality of threads, . . . wherein the first thread is at least associated with a first SCR," and "wherein the step of executing utilizes at least one register file associated with a second thread of the plurality of threads." Thus, claim 7 requires both the plurality of register files and the SCRs to have associated threads. We find that Sollars fails to disclose these limitations for the same reasons discussed above regarding claim 1. Accordingly, we reverse the Examiner's rejection of claim 7 and dependent claim 8 as being anticipated by Sollars.

Claims 16-21

We further note that independent claim 16 recites in pertinent part "setting a first status and control register associated with the first thread and a second status and control register associated with a second thread . . . ." Claim 19 recites "a first status and control register file associated with the first thread," and "a second status and control register associated with a second thread . . . ." Therefore, claims 16 and 19 require that the first and second status and control registers (or status and control register files) must each have associated first and second threads, respectively. As noted *supra*, we find that Sollars fails to disclose these limitations. Accordingly, we reverse the Examiner's rejection of independent claims 16 and 19 and associated dependent claims 17, 18, 20, and 21 as being anticipated by Sollars.

Obviousness rejection of claims 6 and 9

We next consider the Examiner's rejection of claims 6 and 9 as being unpatentable over Sollars. We note that claims 6 and 9 depend from claims 1 and 7, which we have discussed above. We do not conclude, nor does the Examiner establish, that Sollars renders the deficiencies discussed *supra* to be obvious. Accordingly, we find that Appellant has shown that the Examiner erred in rejecting claims 6 and 9. Accordingly, we reverse the Examiner's rejection of claims 6 and 9 as being unpatentable over Sollars.

CONCLUSION

We conclude that Appellant has shown that the Examiner erred in determining that Sollars discloses, teaches, or suggests that the register files and the Status and Control registers correspond to respective threads of the plurality of threads, in the manner claimed.

DECISION

We reverse the Examiner's rejection of claims 1-5, 7, 8, and 16-21 under 35 U.S.C. § 102(b).

We reverse the Examiner's rejection of claims 6 and 9 under 35 U.S.C. § 103(a).

REVERSED

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